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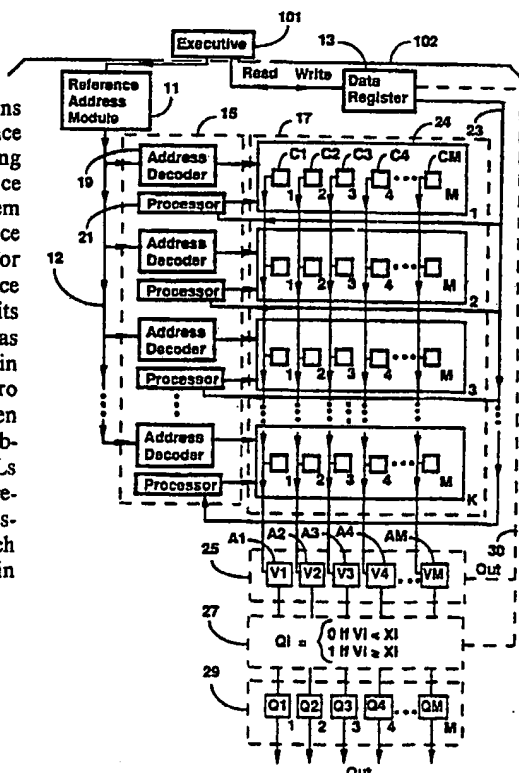
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(54) Title: METHOD AND APPARATUS FOR A SPARSE DISTRIBUTED MEMORY SYSTEM

(57) Abstract

A computer memory system (102) includes k hard memory locations (HMLs) (24), each HML (24) comprising M counters (C1-CM). A reference address element (11) stores a reference address, the reference address being a sequence of N bits. A data register element (13) stores data as a sequence of M integers. In addition, the memory system (102) has a processor system (15) for determining a subset of HMLs (24) to activate for each reference address and for activating those HMLs (24) during reads and writes. For each HML (24), the processor system (15) receives a subset of the reference address bits equal in number to q. The subset of the reference address bits is chosen by selecting, for each HML (24), q integers between 1 and N as selected coordinates (SCs), each SC corresponding to a bit position within the reference address, and for each SC for each HML (24), assigning a zero or one as an assigned value for that SC. The processor system (15) then stores the SCs and the assigned values and in response to receiving the subset of the reference address bits, for each of the SCs for each of the HMLs (24), compares the assigned value for the SC with the value of the corresponding bit in the subset of the reference address bits. The processor system (15) then provides an activation signal for those HMLs (24) for which the assigned values for all SCs are identical with the corresponding bits in the subset of the reference address bits.



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